Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-4 (Withdrawn)

5. (Currently Amended) A method of manufacturing a semiconductor device comprising:

implanting an impurity of a first conductive type in a semiconductor substrate of a second conductive type, wherein the implantation is a single implantation;

~~providing a first gate insulation film on the semiconductor substrate;~~

diffusing the implanted impurity in the substrate through a first gate insulation film formed on the semiconductor substrate by applying a heat treatment, so as to form a first drain region partially under the first gate insulation film and a second drain region adjacent to and above the first drain region, said first drain region having a different impurity concentration than the second drain region, wherein first and second drain regions are formed by a single step of implanting the impurity and forming the first gate insulation by applying heat treatment;

providing a second gate insulation film on the semiconductor substrate except where the first gate insulation film is disposed;

providing a gate electrode that spans from the first gate insulation film to the second gate insulation film;

providing a source region of the first conductive type disposed proximally to one end of said gate electrode; and

providing a third drain region of the first conductive type disposed distally from the other end of said gate electrode and disposed in said second drain region.

6. (Currently Amended) A method for manufacturing a semiconductor device according to Claim 5, wherein ~~providing~~ said first drain region has a lower impurity concentration than the ~~and~~ second drain region ~~comprises diffusing said impurity from the first gate insulation film~~.

7. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 5, further comprising:

providing a layer of the first conductive type to span from one end of said first gate insulation film to said third drain region.

8. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 5, further comprising:

forming a layer of the first conductive type having a high impurity concentration at a predetermined depth in said substrate at a region spanning from a predetermined space from one end of said first gate insulation film to said third drain region, and the high impurity concentration being low at a region near surface of the substrate.

9. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein phosphorus ion is implanted with an energy of about 100 KeV to 200 KeV in the substrate to form the layer.

10. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein phosphorus ion is implanted with an energy of about 100 KeV to 200 KeV in the substrate to form the layer.

11. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein for forming the layer, ion implantation is carried out at a region spanning

from a predetermined space from said first gate insulation film to said third drain region by using a photo-resist as a mask.

12. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein for forming the layer, ion implantation is carried out at a region spanning from a predetermined space from said first gate insulation film to said third drain region by using a photo-resist as a mask.

13. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein for forming the layer, ion implantation is carried out at a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a side wall insulation film formed at a side wall portion of said first gate insulating film as a mask.

14. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein for forming the layer, ion implantation is carried out at a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a side wall insulation film formed at a side wall portion of said first gate insulating film as a mask.

15. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said layer is formed at a region spanning from a predetermined space from the first gate insulation film to said third drain region by using said first gate insulation film as a mask and ion-implanting obliquely from an upper side of the first gate insulation film.

16. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said layer is formed at a region spanning from a predetermined space from the first gate insulation film to said third drain region by using said first gate insulation film as a mask and ion-implanting obliquely from an upper side of the first gate insulation film.

17. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said layer is formed at a region spanning from a predetermined space from the first gate insulation film to said third drain region by using a photo-resist formed to cover said first gate insulation film and ion implanting obliquely from above the first gate insulation film.

18. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said layer is formed at a region spanning from a predetermined space from the first gate insulation film to said third drain region by forming a photo-resist formed to cover said first gate insulation film and ion implanting obliquely from above the first gate insulation film.

19. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 7, wherein said first drain region has a lower impurity concentration than said second drain region.

20. (Previously Presented) A method of manufacturing a semiconductor device according to Claim 8, wherein said first drain region has a lower impurity concentration than said second drain region.